Introduction

This volume is organized into seven sections: (1) Standards for Semiconductor Industry; (2) Epitaxial Technology; (3) Dielectrics and Junction Formation Techniques; (4) Plasma Technology and Other Fabrication Techniques; (5) Material Defects, Oxygen and Carbon in Silicon; (6) Yield Enhancement and Contamination Control Aspects; (7) Dopant Profiling Techniques and In-Process Measurements; and (8) Fab Equipment: Automation and Reliability. The papers describe the emerging semiconductor processes used in device fabrication, from its simplest use to discrete circuits through the complex applications to very-large-scale-integrated (VLSI) circuits.

After the introduction, unedited excerpts of one keynote paper, "Silicon and Semiconductors: Partners in the Late 1980's" are given. The synopses on workshops and graduate education are presented in two appendixes, I & II at the end of the volume.

STANDARDS FOR SEMICONDUCTOR INDUSTRY

Quality of measurement is the cornerstone of ASTM's system for the development of voluntary consensus standards. From the inception of the test method, through balloting and interlaboratory testing, the volunteers assure a high level of precision. The standard test methods, nomenclature, and specifications developed by ASTM and SEMI for the semiconductor industry support many acceptance tests and online measurements. The history of this collaborative work and its expected future course is discussed in this paper. The standards activities of foreign organizations and the interactions among these groups are also discussed.

EPITAXIAL TECHNOLOGY

The epitaxial layer is a backbone of the device structure. Major emphasis in epitaxial technology is to lower the defect level and improve the dopant distribution within the layer. The papers in this section discuss various techniques to improve epilayer quality. R. Reif presents a low pressure CVD system to deposit epitaxial films both with and without plasma enhancement at temperatures as low as 650°C. Chang and Rosczak adopt a more conventional atmospheric CVD system at 825°C to deposit epitaxial films. Swaroop and Fisher, et al present methods to improve epitaxial quality with respect to as-grown defects and electrical
parameters. Medernach and Wells study the vapor etch, and Wong et al present methods to improve the epilayer quality using intrinsic gettering techniques.

**DIELECTRICS AND JUNCTION FORMATION TECHNIQUES**

Deposition and properties of ultra-thin dielectric insulators are presented by S. Roberts and others. Various aspects of both, the conventional and implantation techniques for junction formation are discussed. These include doped oxide spin-on source diffusion, and measurement of cross-contamination levels produced during implantation. The ion beam nitridation and a CVD reactor (productivity model) are also given in this section.

**PLASMA TECHNOLOGY AND OTHER FABRICATION TECHNIQUES**

A wide variety of plasma technology issues are presented in six papers. The topics of these papers include: RIE damage, bonding structure and chemical analysis of PECVD and LPCVD dielectric films, plasma etch emission endpoint, profile control, quality control and optimization during plasma deposition. Also presented in this section are the effects of UV radiation on photoresist in Al etch and palladium silicide contact process.

**MATERIAL DEFECTS, OXYGEN AND CARBON IN SILICON**

Material defects may be classified in various categories: bulk defects, surface defects, process-induced defects, deep levels, gettered impurities etc. Most of these categories are discussed in the papers in this section. Liaw et al and Rose suggest the use of wafer scanners to screen the incoming wafers for defects. Dyer discusses many defects introduced in ingot-to-wafer processing which may lead to device degradation. Shiraiwa and Inenaga explain the haze on wafers. The haze may be due to silicon oxide nodules which grow on the silicon surface in the density of about 1000 to 10 000 per square centimeter. Arst describes a laser-induced mass analysis technique to identify impurities captured in defect structures. Suga and Murai discuss the effects of bulk defects on the intrinsic and extrinsic gettering in silicon.

**YIELD ENHANCEMENT AND CONTAMINATION CONTROL ASPECTS**

Device yields are dependent upon a number of factors. Processing defects, variability in fabrication, and contamination during device processing are just a few factors which can impact the device yields. These
aspects are discussed in this section. Kar and Tewari attempt to identify the nature of defects induced by e-beam evaporation at the silicon-oxide interface. Maass describes the application of the Generation of Moments method and relates device parameters to processing variables. He shows that tightening the distributions of key device parameters results in an enhancement and prediction of yields. Beck explains that an overall circuit yield is the product of two independent factors, namely, the device physics limitations yield factor and the process defect loss yield factor. The papers on contamination control emphasize the following points: the need to provide a clean environment for fabrication including ultra clean SMIF boxes, dedicated robotic mechanisms and clean air equipment enclosures, particulate control on the wafers and in gases and chemicals.

DOPANT PROFILING TECHNIQUES AND IN-PROCESS MEASUREMENTS

A number of papers were presented on the dopant profiling techniques. These techniques included SIMS, Rutherford backscatter, spreading resistance, and capacitance-voltage. These papers are listed in this section. A workshop was also held on this topic. The synopsis of workshop is given in appendix I.

FAB EQUIPMENT: AUTOMATION AND RELIABILITY

Computer-aided Manufacturing [CAM] and Computerized Integrated Manufacturing [CIM] are discussed in detail in this section. The development of a flexible wafer fab automation system is described. The latter performs three basic functions, real-time inventory control, material distribution throughout the fab, and automated loading of cassette-to-cassette process equipments.

In as much as the automation and mechanization are essential to the future of our industry, so is the understanding of both, the raw capability of each component of a system and the capability of each component with human factors integrated. The paper by Greiner isolates and defines components of real factory time and formulates them in two distinct ways: with and without human interfacing. This paper is the result of a SEMI document, presently in preparation by the SEMI Standards Committee.

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